into the inside from a surface of the second interlayer insulating film 21 to prevent the penetration of the moisture. In the following, this process is called the N_2O plasma process. In this embodiment, 350 ℃ and 2 minutes, for example, are selected as the annealing temperature and the annealing time respectively.

Next, steps for forming the structure shown in FIG.7 will be explained hereunder.

First, first contact holes 21a are formed in the second interlayer insulating film 21 on the upper electrodes ~~16a~~ 18a of the ferroelectric capacitors 20 by the photolithography method. At the same time, contact holes (not shown) are formed on the contact areas of the lower electrodes, which are arranged in the direction perpendicular to this sheet of FIG.7. Then, the recovery annealing is applied to the dielectric films 17a. Specifically, the dielectric films 17a are annealed at the temperature of 550 ℃ for 60 minute in the oxygen atmosphere.

Then, the second interlayer insulating film 21, the SiO_2 film 15, and the SiON film 14 are patterned by the photolithography method. Thus, second contact holes 21b are formed on the second conductive plugs 13b, which are located near both ends of the p-well 3 in the memory cell region A, respectively to expose the second conductive plugs 13b. Then, a TiN film of 125 nm thickness is formed on the second interlayer insulating film 21 and in the

ABSTRACT OF THE DISCLOSURE

There is provided a semiconductor device which ~~comprises~~ includes a first interlayer insulating film (first insulating film) formed over a silicon (semiconductor) substrate, a capacitor formed on the first interlayer insulating film and having a lower electrode, a dielectric film, and an upper electrode, a fourth interlayer insulating film (second insulating film) formed over the capacitor and the first interlayer insulating film, and a metal pattern formed on the fourth interlayer insulating film over the capacitor and its periphery to have a stress in an opposite direction to the fourth interlayer insulating film. As a result, characteristics of the capacitor covered with the interlayer insulating film can be improved.

What is claimed is:

1. A semiconductor device comprising:

a first insulating film formed over a semiconductor substrate;

a capacitor formed on the first insulating film and having a lower electrode, a dielectric film, and an upper electrode;

a second insulating film formed over the capacitor and the first insulating film; and

a metal pattern formed on the second insulating film over the capacitor and a periphery thereof, and having a stress in an opposite direction to a stress of the second insulating film.

2. The semiconductor device according to claim 1, further including metal wiring patterns formed in the second insulating film.

3. A semiconductor device comprising:

a first insulating film formed over a semiconductor substrate;

a capacitor formed on the first insulating film and having a lower electrode, a dielectric film, and an upper electrode;

a second insulating film formed over the capacitor and the first insulating film;

a recess formed in the second insulating film over the capacitor and a periphery thereof; and

a metal pattern formed in the recess and having a

stress in an opposite direction to a stress of the second insulating film.

4. The semiconductor device according to claim 1, wherein a potential of the metal pattern is a fixed potential or a floating potential.

5. The semiconductor device according to claim 1, wherein the capacitor is formed in plural in a cell region, and the metal pattern covers an entirety of the cell region.

6. The semiconductor device according to claim 5, wherein the metal pattern is formed wider than the cell region.

7. The semiconductor device according to claim 1, wherein the stress of the metal pattern is a tensile stress.

8. The semiconductor device according to claim 1, wherein the metal pattern is formed to have a single-layer structure or a multi-layered structure.

9. The semiconductor device according to claim 1, wherein the metal pattern is made of any material selected from the group consisting of aluminum, titanium, copper, tantalum, and tungsten, or made of material containing any one selected from the group consisting of aluminum, titanium, copper, tantalum, and tungsten.

10. A manufacturing method of semiconductor device comprising:

forming a first insulating film over a semiconductor substrate;

forming capacitors, each having a lower electrode, a